WHAT IS CLAIMED IS:

1. A nonvolatile memory apparatus comprising:

a control circuit;

a plurality of terminals including a clock terminal, a command terminal and other terminal;

a clock generator; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a first clock signal,

wherein said command terminal receives commands which comprise a read command and a program command,

wherein said clock generator is controlled by said control circuit for generating a second clock signal,

wherein said control circuit reads out operation steps from a program memory for controlling an operation of a received command by executing said operation steps,

wherein in an operation in response to said read command received from said command terminal, said control circuit controls, based on operation steps corresponding to said read command, reading data from ones of said nonvolatile memory cells, and outputting data via said other terminal not said command terminal in response to said first clock signal,

wherein in an operation in response to said program command received from said command terminal, said control circuit controls, based on operation steps corresponding to said program command, receiving data via said other terminal not said command terminal in response to said first clock signal, and writing data to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

2. A nonvolatile memory apparatus according to claim 1, wherein in said operation in response to said program command, said control circuit further controls a verify operation for verifying whether each of ones of said nonvolatile memory cells completes writing data or not.

3. A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state and keeping threshold voltages of remaining nonvolatile memory cells of ones of said nonvolatile memory cells within said threshold voltage range indicating said erase state based on said operation steps corresponding to said program command.

4. A nonvolatile memory apparatus according to claim 3, wherein said commands further comprising:

an erase command,

wherein in an operation in response to said erase command received

from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state based on said operation steps in response to said erase command.

5. A nonvolatile memory apparatus according to claim 4, wherein said control circuit comprises:

a circuit, and

wherein in said operation in response to said read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

6. A nonvolatile memory apparatus according to claim 5, wherein said other terminal is a data terminal,

wherein in said operation in response to said program command, said data terminal is capable of receiving data in response to said first clock signal, and

wherein in said operation in response to said read command, said data terminal is capable of outputting data in response to said first clock signal.

7. A nonvolatile memory apparatus according to claim 1, wherein

said control circuit has said program memory therein.

8. A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state, and

wherein in said operation in response to said program command, said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating said program states according to data and keeping threshold voltages of remaining nonvolatile memory cells of ones of said nonvolatile memory cells.

9. A nonvolatile memory apparatus according to claim 8, wherein said commands further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state based on said operation steps

corresponding to said erase command.

10. A nonvolatile memory apparatus according to claim 9, wherein said control circuit comprises:

a circuit, and

wherein in said operation in response to said read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or any one of said threshold voltage ranges indicating said program state.

11. A nonvolatile memory apparatus according to claim 10, wherein said other terminal is a data terminal,

wherein in said operation in response to said program command, said data terminal is capable of receiving data in response to said first clock signal, and

wherein in said operation in response to said read command, said data terminal is capable of outputting data in response to said first clock signal.

12. A nonvolatile memory apparatus comprising:

a control circuit:

a clock generator;

a clock terminal;

a data terminal;

a command terminal; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a first clock signal,

wherein said data terminal receives data in response to said first clock signal and outputs data in response to said first clock signal,

wherein said command terminal receives commands which includes a read command and a program command,

wherein said clock generator is controlled by said control circuit for generating a second clock signal,

wherein said control circuit executes operation steps corresponding to a received command read out from a program memory,

wherein in an operation in response to said read command received from said command terminal, said control circuit controls, based on operation steps corresponding to said read command, reading data from ones of said nonvolatile memory cells, and serially outputting data via said data terminal in response to said first clock signal,

wherein in an operation in response to said program command received from said command terminal, said control circuit controls, based on operation steps corresponding to said program command, serially receiving data via said data terminal in response to said first clock signal and writing data to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

13. A nonvolatile memory apparatus according to claim 12, wherein in said operation in response to said program command, said control circuit

controls a verify operation for verifying whether each of ones nonvolatile memory cells completes writing data or not.

14. A nonvolatile memory apparatus according to claim 13, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state, and keeping threshold voltages of remaining memory cells of ones of said nonvolatile memory cells within said threshold voltage range indicating said erase state based on said operation steps corresponding to said program command.

15. A nonvolatile memory apparatus according to claim 14, wherein said commands further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltages of ones of nonvolatile memory cells to within said threshold

voltage range indicating said erase state based on said operation steps corresponding to said erase command.

16. A nonvolatile memory apparatus according to claim 15, wherein said control circuit comprises:

a circuit, and

wherein in said operation in response to read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

17. A nonvolatile memory apparatus according to claim 12, wherein said control circuit has said program memory therein.

18. A nonvolatile memory apparatus according to claim 13, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state,

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating said program states according to data, and keeping said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells based on said operation steps corresponding to

said program command.

19. A nonvolatile memory apparatus according to claim 18, wherein said commands further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state based on said operation steps corresponding to said erase command.